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FOR

METHOD OF IMPROVING ADHESION BETWEEN TWO DIELECTRIC FILMS

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METHOD OF IMPROVING ADHESION BETWEEN TWO DIELECTRIC FILMS

Background Of The Invention

1. Field of the Invention

The present invention relates to manufacturing of integrated circuits on semiconductor substrates and, in particular, to a method of improving adhesion between an insulating layer and a cap layer within such integrated circuits.

2. Description of Related Art

In semiconductor fabrication processes, layers of insulating, conducting and semiconductor materials are commonly deposited and patterned to form integrated circuits (IC). These multilayer electronic components may further be provided with contact vias and line wirings formed in the insulating materials of such ICs, which, are referred to as interlevel dielectrics (ILDs). Typically, ILDs are made by damascene and dual damascene processing techniques.

In damascene processing, multilayer electronic components are made by depositing a dielectric material on a surface of a substrate to form an insulating layer and then patterning the insulating layer to form openings for trenches therein such insulating layer. Once trenches are formed, a conductive material is deposited into the trenches and then any excess conductive material may be removed from the structure surface to form damascene regions within the insulator layer.

Dual damascene processing similarly involves etching trenches within the insulating layer of the IC and further etching vias at the bottom of these trenches. In ICs where contact vias also extend downwardly from the bottom of the trenches, both the trenches and the downwardly extending vias are simultaneously filled with

conductive material. This process forms both contact vias and integrated wires for interconnecting electrical devices and wiring at various levels within the IC.

Thus, in the process of forming multilayer electronic components, using both damascene and dual damascene processes, several layers are required to form the contact vias and integrated wires. For example, a typical multilayer electronic component may be built up from a first insulating layer on a substrate by forming an opening therein and then filling the opening with a conductive fill material to form conductive lines. However, prior to metallization, a barrier layer is typically provided within the openings in the first insulating layer to avoid metal diffusion between the conductive fill and the first insulating layer.

A second insulating layer is deposited over the first insulating layer and the metallization. Trenches and contact vias are then formed in this second insulating layer to form the line wirings and contact vias of the multilayer electronic component. Again, prior to metallization, a barrier layer may be deposited into the trenches and vias so as to coat the sidewalls of the openings in order to prevent any metal diffusion. The trenches and vias are then filled with metallization and the surface area of the substrate planarized, such as, by chemical mechanical polishing.

However, during the polishing process, the barrier layer may delaminate from the insulating layer resulting in interruption of polishing process as well as damage to the multilayer electronic component. This delamination problem is particularly severe in those devices having low k dielectric constant insulating layers. One method to decrease the problem of delamination between low k dielectric constant insulating layers and barrier layers has been to deposit a cap

layer between the insulating layer and the barrier layer. However, the use of cap layers is ineffective as delamination occurs between the insulating and cap layers, and in particular, between low k dielectric constant insulating layers and cap layers.

Therefore, a need exists in the art for preventing delamination between insulating layers and cap layers, particularly, those insulating and cap layers used in single and dual damascene processes.

Summary of the Invention

Bearing in mind the problems and deficiencies of the prior art, it is therefore an object of the present invention to provide a method for preventing delamination between insulating layers and cap layers.

Another aspect of the invention is to provide a method for providing improved adhesion between insulating layers, preferably low k dielectric constant insulating layers, and cap layers in single and dual damascene processes.

It is another object of the present invention to provide uniquely modified damascene and dual damascene processes for fabricating multilayer electronic components.

Yet another aspect of the invention is to provide multilayer electronic components made using the method of the invention.

Still other objects and advantages of the invention will in part be obvious and will in part be apparent from the specification.

The above and other objects, which will be apparent to those skilled in art, are achieved in the present invention, which, is directed to in a first aspect a

method of improving adhesion between an insulating layer and a capping layer in a process for making electronic components.

The method includes providing an integrated circuit structure which is in the process of being fabricated into a finished electronic component having an insulating layer. An exposed surface of the insulating layer is contacted with a gas for adsorption of such gas onto the exposed surface to form a treated surface area of the insulating layer while simultaneously maintaining an original thickness of the insulating layer. A capping layer is deposited over the treated surface area and then the process of making the integrated circuit device continues, wherein the treated surface area improves adhesion between the insulating layers and the capping layer to prevent delamination therebetween during these subsequent processing steps.

Preferably, the insulating layer has a thickness ranging from about 2,000 Å to about 10,000 Å, and comprises a low k dielectric, such as, organo silicate glass, polyimide, organic siloxane polymer, polyarylene ether, nano-porous silica, hydrogen silesquioxane glass and methyl silesquioxane glass.

In this first aspect, the gas is preferably silane, disilane, dichlorosilane, germane and combinations thereof, whereby the adsorbed gaseous particles may include molecules, radicals, derivatives and combinations thereof. In adsorption of such gaseous particles onto the surface of the insulating layer, it is critical that the insulating layer and substrate be heated, preferably to a temperature ranging from about 100°C to about 500°C and then the gas is flown over these heated surfaces for adsorption thereon. This may be accomplished at a pressure ranging from about 0.5 Torr to about 10 Torr and for a duration of about 50 sccm to about 500 sccm.

In a second aspect, the invention is directed to a method of forming a semiconductor device by providing a substrate layer, depositing an insulating layer thereon and then heating the substrate layer and the insulating layer. Once heated, the treatment gas is flown over a surface of the heated insulating layer.

In so doing, this treatment gas contacts the heated surface for adsorption of the gas onto the surface of the insulating layer to form a treated surface area thereof while maintaining an original thickness of the insulating layer. A capping layer is then deposited directly over the insulating layer wherein the treated surface area of the insulating layer improves adhesion between the insulating and the capping layers to prevent delamination therebetween during subsequent processing steps

In a third aspect, the invention is directed to an intermediate semiconductor structure. This intermediate semiconductor structure includes a substrate layer, an insulator layer disposed over the substrate layer having a treated surface area comprising adsorbed gaseous particles and a capping layer disposed over the treated surface area of the insulator layer. In accordance with the invention, the treated surface area of this intermediate structure advantageously prevents any delamination between the insulator layer and the capping layer.

Brief Description of the Drawings

The features of the invention believed to be novel and the elements characteristic of the invention are set forth with particularity in the appended claims. The figures are for illustration purposes only and are not drawn to scale. The invention itself, however, both as to organization and method of operation,

may best be understood by reference to the detailed description which follows taken in conjunction with the accompanying drawings in which:

Fig. 1 is a cross-sectional view of a substrate processed in accordance with the invention having a treated surface area of an insulating layer.

Fig. 2 is a cross-sectional view of the structure of Fig. 1 showing the step of forming openings in a mask over a surface of a capping layer.

Fig. 3 is a cross-sectional view of the structure of Fig. 2 showing the step of transferring the openings of the mask into the underlying structure to form openings therein with exposed surfaces of a dielectric layer.

Fig. 4 is a cross-sectional view showing the step of removing the mask of Figs. 3 and 4.

Fig. 5 is a cross-sectional view of the structure of Fig. 4 showing the step of filling the openings with a photo resist material.

Fig. 6 is a cross-sectional view of the structure of Fig. 5 showing the step of recessing back the photo resist material to form a photo resist plug within each of the openings in the structure.

Fig. 7 is a cross-sectional view of the step of forming a second mask over the structure of Fig. 6 for forming trenches within such intermediate semiconductor structure.

Fig. 8 is a cross-sectional view of the step of forming such trenches within such intermediate semiconductor structure of Fig. 7.

Fig. 9 is a cross-sectional view of the structure of Fig. 8 showing the step of removing the second mask, the photo resist plug within each via, as well as the exposed dielectric layer within each via.

Fig. 10 is a cross-sectional view showing the step of forming metallization layers within the trenches and vias of the structure of Fig. 9.

Fig. 11 is a cross-sectional view showing the step of planarizing the structure of Fig. 10 whereby in accordance with the invention the treated surface area of the insulating layer significantly prevents any delamination from occurring between such insulating layer and a capping layer directly thereover.

Description of the Preferred Embodiment(s)

In describing the preferred embodiment of the present invention, reference will be made herein to Figs. 1-11 of the drawings in which like numerals refer to like features of the invention.

The present invention overcomes problems of delamination between a capping layer and an insulating layer in fabrication of a semiconductor device. Advantageously, the invention provides a method of forming a semiconductor device, and the semiconductor device fabricated using such method, that significantly improves adhesion between capping and insulator layers, which in turn, prevents any delamination from occurring between such layers during further processing of the semiconductor device, particularly during subsequent planarization processes. These steps may be repeated a number of times on the

substrate to complete the fabrication of the semiconductor device. The invention will be better understood with reference to the drawings.

Referring to Fig. 1, a substrate 10 is provided, which, preferably includes insulator regions 12 of a known insulator material and metal regions 14 fabricated by known techniques. The substrate 10 may comprise any known substrate material including, but not limited to, Si_3N_4, SiC, low k dielectric SiO_2, doped SiO_2. A first dielectric layer 20 is then deposited directly over the substrate 10. This first dielectric layer 20 may include a material, such as a low k dielectric constant interlevel dielectric material, SiC, SiN and the like, deposited to a thickness ranging from about 300 Å to about 800 Å by known techniques.

Next, an insulating layer 30 is deposited directly over the first dielectric layer 20 to a thickness ranging from about 2000Å to about 10,000Å also by known techniques. In accordance with the invention, the insulating layer 30 preferably comprises any known low k dielectric material including, but not limited to, CORAL™ of Novellus Systems, Inc., BLACK DIAMOND™ of Applied Materials, Inc., SiLK™ of Dow Corning, Inc., NANOGLASS™ of Nanopore, Inc, and the like. Other low k dielectric materials used to form insulating layer 30 may include, for example, organo silicate glass, polyimide, organic siloxane polymer, polyarylene ether, methyle hydrogen, nano-porous silica, hydrogen silesquioxane glass and methyl silesquioxane glass.

Once the insulating layer 30 is deposited on the first dielectric layer 20, the surface area of insulating layer 30 is treated to form a treated surface area 35 of

insulating layer 30 for improving adhesion between such insulating layer 30 and a subsequently deposited capping layer 40.

In forming the treated surface area 35 of insulating layer 30, once the insulating layer 30 is deposited, the structure is treated in a gaseous environment, within a treatment chamber, at an elevated temperature for a duration sufficient for adsorption of such gas particles, radicals, or derivatives thereof onto the exposed surface areas of the insulating layer 30. Preferably, the insulating layer 30 is treated in chemical vapor deposition chamber. In accordance with the invention, the treatment gas is continually flown into the treatment chamber over the exposed surface areas of insulating layer 30 during the formation of treated surface area 35. In so doing, the treated surface area 35 is formed only at exposed surface areas of insulating layer 30 whereby the insulating layer 30 maintains its original thickness. This, is a critical feature of the invention as the treated surface area 35 of insulating layer 30 improves adhesion between such insulating layer 30 and a subsequently deposited capping layer without requiring any additional height or architecture to the structure 10, 20, 30; particularly to insulating layer 30.

In more detail, in treating the insulating layer 30, the treatment chamber is preferably preheated and maintained at a temperature ranging from about 100°C to about 500°C. The substrate having the insulating layer thereover is then provided within the preheated chamber and also heated to a predetermined temperature ranging from about 100°C to about 500°C, preferably at about 400°C. The substrate 10, 20 having insulating layer 30, preferably of a low k dielectric

insulating material, is maintained at this temperature during the formation of the treated surface area 35.

Once the structure is maintained at the predetermined temperature, the treatment gas is flown into the treatment chamber at a pressure ranging from about 0.5 Torr to about 10 Torr over the insulating layer 30 while maintaining the structure at the predetermined temperature. The treatment gas preferably comprises a silane-based or germanium-based gas, such as, silane, disilane, dichlorosilane, germane, and combinations thereof. In accordance with the invention, it is critical that the treatment gas be a reactive in nature, such as, those used for film depositions.

In the preferred embodiment the treatment gas comprises silane gas flown over surfaces of a low k insulating layer 30. The gas is continually flown into the treatment chamber over the insulating layer 30 for a sufficient duration that allows the adsorption of the gaseous particles, radicals or derivatives onto the exposed surfaces of insulating layer 30 to form the treated surface area 35. Preferably, the gas is continually flown into the treatment chamber over exposed surfaces of insulating layer 30 for a time ranging from about 50 sccm to about 500 sccm.

Subsequently, the adsorbed gaseous particles, molecules, radicals or derivatives of the treated surface area 35 may then optionally undergo an oxidation or carbonization process. This may be accomplished by flowing an oxygen-based gas or carbon-based gas including, but not limited to, CH_4, CO_2, O_2 or combinations thereof, over the treated surface area 35 in order to oxidize and/or carbonize the adsorbed gases of the treated surface area 35. The nitridization or

carbonization process can be performed using a plasma process with a power in the range of about 100 W to about 1000 W.

Once the treated surface area 35 of insulating layer 30 is formed, and optionally oxidized and/or carbonized, a capping layer 40 is provided directly and entirely over this treated surface area 35, whereby the treated surface area 35 of the invention significantly improves adhesion between it and the capping layer 40. The capping layer 40 may be comprise a material including, but not limited to, silicon oxide, silicon carbide, silicon nitride, and the like, deposited by known techniques to a thickness ranging from about 2 nm to about 100 nm.

Referring to Fig. 2, once the capping layer 40 is deposited over the treated surface 35 of insulating layer 30 the structure is further processed, wherein during such subsequent processing steps the improved adhesion between the insulating layer 30 and the capping layer 40 as a result of treated surface area 35 substantially prevents any delamination from occurring between such layers during these further processing steps.

In accordance with the invention, the semiconductor device is further processed by forming mask 50 over a surface of capping layer 40 by a known technique. As shown in Fig. 2, the mask 50 is patterned and exposed, preferably via lithography, to form openings 52 therein mask 50. Referring to the dashed lines 54 in Fig. 2, the openings 52 of mask 50 are then transferred into the underlying substrate.

Referring to Figs. 3 and 4, openings 52 of mask 50 are transferred into the underlying structure by etching through correlating regions of sequentially exposed

capping layer 40, treated area 35 and the insulating layer 30, stopping at a top surface of the first dielectric layer 20 to form openings 60. Remaining portions of mask 50 are then removed, preferably by a photo resist dry stripping technique, to expose a top surface of the capping layer 40 as shown in Fig. 4. The exposed surface areas of this resultant structure as shown in Fig. 4 are then cleaned, preferably via a wet clean technique.

Once the surfaces of the intermediate structure are cleaned, a photo resist layer 70 is deposited over the structure surface in an amount sufficient to at least fill the openings 60 as shown in Fig. 5. Preferably, the photo resist layer 70 may be deposited by an I-line resist coating technique. The photo resist layer 70 is then etched back to a sufficient depth so as to leave remaining portions of photo resist layer within openings or vias 60. Referring to Fig. 6, the photo resist layer 70 is preferably etched back so as to leave remaining photo resist plugs 72 within vias 60 whereby the capping layer 40 remains exposed at a surface of this resultant intermediate structure. This may be accomplished by an I-line resist etch technique.

The structure of Fig. 6 may be further processed in accordance with the present dual damascene processing technique. In so doing, a second mask 80 is formed over the structure as shown in Fig. 6 by initially depositing a photo resist material over the surface followed by patterning and exposing such resist layer, preferably via lithography, to form openings 82 as shown in Fig. 7.

Openings 82 are used to form trenches within the semiconductor structure. In so doing, the openings 82 are formed directly over locations of openings 60. In

accordance with the invention, these openings 82 may be the same size as openings 60, or alternatively as shown in Fig. 7, these openings 82 may be larger in dimension in comparison to openings 60. As shown by the dashed lines in Fig. 7, the openings 82 are transferred into the remaining portions of underlying capping layer 40, treated surface 35 and insulating layer 30 by etching there-through such layers stopping at a distance within the insulating layer 30 as shown in Fig. 8. This may be accomplished by line etching these layers to a depth ranging from about 2,000 Å to about 5,000 Å.

Referring to Fig. 9, once openings 82 are transferred into the underlying structure, the second mask 80 is removed, preferably by a photo resist dry strip process, therein exposing a top surface of the capping layer 40 and removing any photo resist plug 72 remaining within vias 60, as well as any subsequently exposed regions of the first dielectric layer 20 at the bottom of vias 60. The resultant structure is cleaned, preferably via a wet clean process, to form trench 85 openings overlying via 65 openings and having exposed regions of the metal region 14 of the substrate 10. Subsequently, the structure of Fig. 9 may be provided with metallization layers whereby the treated surface area 35 prevents delamination between the insulating layer 30 and the capping layer 40 during such processing steps.

Referring to Fig. 10, the exposed surfaces of the structure are cleaned and then a barrier layer 92 is deposited entirely over all exposed surfaces of the structure whereby the barrier layer 92 directly contacts the exposed metal portions 14 of the substrate at the bottom of via 65 openings. The barrier layer may include

a known refractory metal (Ta, Ti, W), refractory metal nitrides (TaN, TiN, WN), refractory metal alloys (TaSiN), or combinations thereof deposited to a thickness of about 2 nm to about 100 nm by known techniques, such as, by physical vapor deposition. Once the barrier layer 92 is deposited, a seed layer 94 may be deposited directly and entirely over the barrier layer 92. The seed layer 94 may comprise a copper seed layer also deposited to a thickness ranging from about 500 Å to about 2000 Å by known techniques, such as, sputtering and chemical vapor deposition.

After the barrier layer 92 and the seed layers 94 are deposited, remaining portions within vias 65 and trenches 85 are filled with a conductive material 96. The conductive material of this metallization layer 96 may comprise a metal. Preferably, the metallization layer is a copper electrofill layer, which once deposited, is subjected to a known annealing technique.

Upon completion of deposition of the metallization layer 96, the surface of the structure of Fig. 10 is planarized whereby the capping layer 40 may be removed, may be partially removed, or alternatively may remain on the surface of the substrate. This planarization step forms conductive features 100 that isolated from adjacent conductive features via insulating layer 30. The planarization may be accomplished by known chemical mechanical polishing techniques such as, for example, an abrasive-free polishing technique. Subsequently, the seed layer and the barrier layers are planarized to expose surfaces of the capping layer 40 as shown in Fig. 11. This too may be accomplished by known chemical mechanical polishing techniques. During this planarization process, a critical feature of the

invention is that the treated surface area 35 of the low k insulating layer 30 substantially prevents any delamination from occurring between such low k dielectric constant insulating layer 30 and the overlying capping layer 40.

As will be understood in accordance with the invention, the instant method may be used to form a variety of semiconductor surfaces requiring strong adhesion between an insulating layer, particularly a low k dielectric insulating layer, and an overlying capping layer, particularly an oxide layer. These semiconductor surfaces include, but are not limited to, planarized multi-level metal interconnect structures, planarized shallow trench isolation structures, planarized semiconductor islands, and a variety of other surfaces as known and used in the art.

For example, the invention is useful in fabricating integrated circuits that require the use of a trench etch stop layer. In these circuits, a first dielectric layer is deposited over the substrate. Exposed surface areas of this first dielectric layer are then provided with the treated surface area of the invention by flowing a gas over the surface for adsorption of such gaseous particles onto the exposed surfaces of the first dielectric. After this treatment step, an etch stop layer is directly deposited over the treated surface area of the insulating dielectric layer whereby the treated surface improves adhesion between the etch stop layer and the treated first dielectric layer. The etch stop layer may comprise a trench etch stop layer comprising a material including but not limited to a SiN, SiC and the like.

Subsequently, exposed surface areas of the etch stop layer may also undergo the treatment process of the invention to form treated surface areas of the etch stop for improving adhesion between such etch stop layer and a subsequently deposited

second dielectric layer. The improved adhesion is a result of the adsorbed gaseous particles on the surface of the etch stop layer. This second dielectric layer over the etch stop layer may also be subjected to the treatment process of the invention to form adsorbed gaseous particles on the surface of the second dielectric layer. These adsorbed gaseous particles on the second dielectric layer improve adhesion between this second dielectric layer and a subsequently deposited capping layer.

Thus, in accordance with the present invention, an essential feature is that the treated surface area 35 comprising adsorbed gaseous particles on surfaces of the insulating layer significantly improves adhesion between such insulating layer and another layer deposited directly over the treated surface area, which in turn, eliminates delamination from occurring between such layers during further processing of the integrated circuit, particularly during planarization processes.

While the present invention has been particularly described, in conjunction with a specific preferred embodiment, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art in light of the foregoing description. It is therefore contemplated that the appended claims will embrace any such alternatives, modifications and variations as falling within the true scope and spirit of the present invention.

Thus, having described the invention, what is claimed is: